NASCOM FLOAT AND STEP

DISPLAY TESTER

MK. III

PURCHASING AND PCB DESIGN INFORMATION.

DISTRIBUTION: P.C.B. LAYOUT DESIGNER (WITH ORIG. PHOTO'S AND MK.II PROTOTYPE).

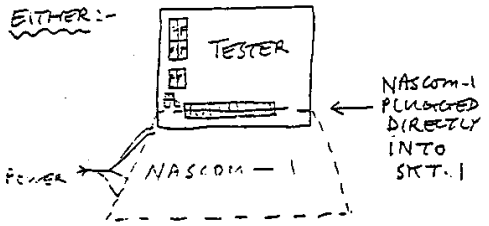
D.R. Wadham.

30.10.78.

ISSUE 2 : AMENDED TO 14.5.79.

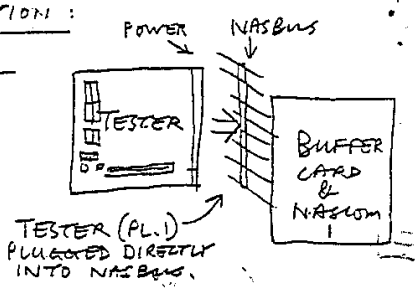
ALTERNATIVE METHODS OF OPERATION :

EITHER :-



TO TEST NASCOM-1 CPU BOARD ALONE

OR : —



TO TEST NASBUS, BUFFER CARD AND NASCOM-1

FACILITIES PROVIDED (IN OUTLINE).

ADDRESS BUS (A0-A15) → TEST POINTS → 4 HEXADECIMAL DISPLAYS.

DATA BUS (D0-D7) → TEST POINTS → 2 HEXADECIMAL DISPLAYS. (+PROVISION FOR 2 MORE FOR D8-D15 IF REQUIRED IN FUTURE)

TRISTATED CONTROLS → TEST POINTS → 4 DECIMAL POINTS IN DISPLAYS

OTHER CONTROLS → 8 DECIMAL POINTS IN DISPLAYS

RESET PUSH BUTTON.

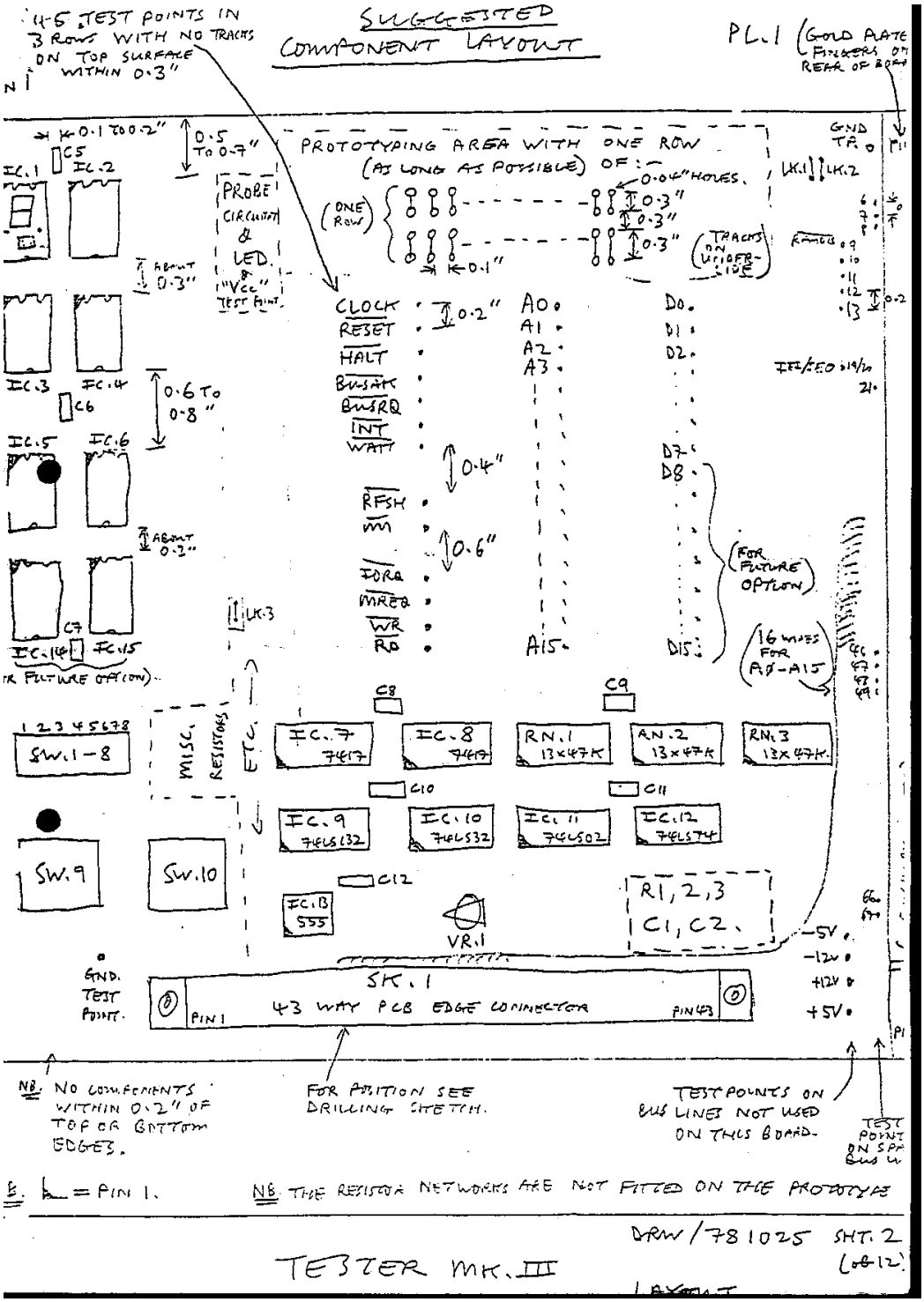
STEP PUSH BUTTON (REMOVES WAIT STATE FOR 1 CLOCK CYCLE)

8 MODE CONTROL SWITCHES :

BUS REQUEST, RUN/STEP, STOP ON M1 CYCLES ONLY, SKIP MEMORY CYCLES, SKIP READ CYCLES, AUTO REPEAT, SLOW/FAST, HOLD DISPLAY (AT AN ARBITRARY TIME).

VARIABLE AUTO REPEAT RATE.

PROBE TO TEST FLOATING LINES (WITH WARNING LED IF LINE HELD HIGH).



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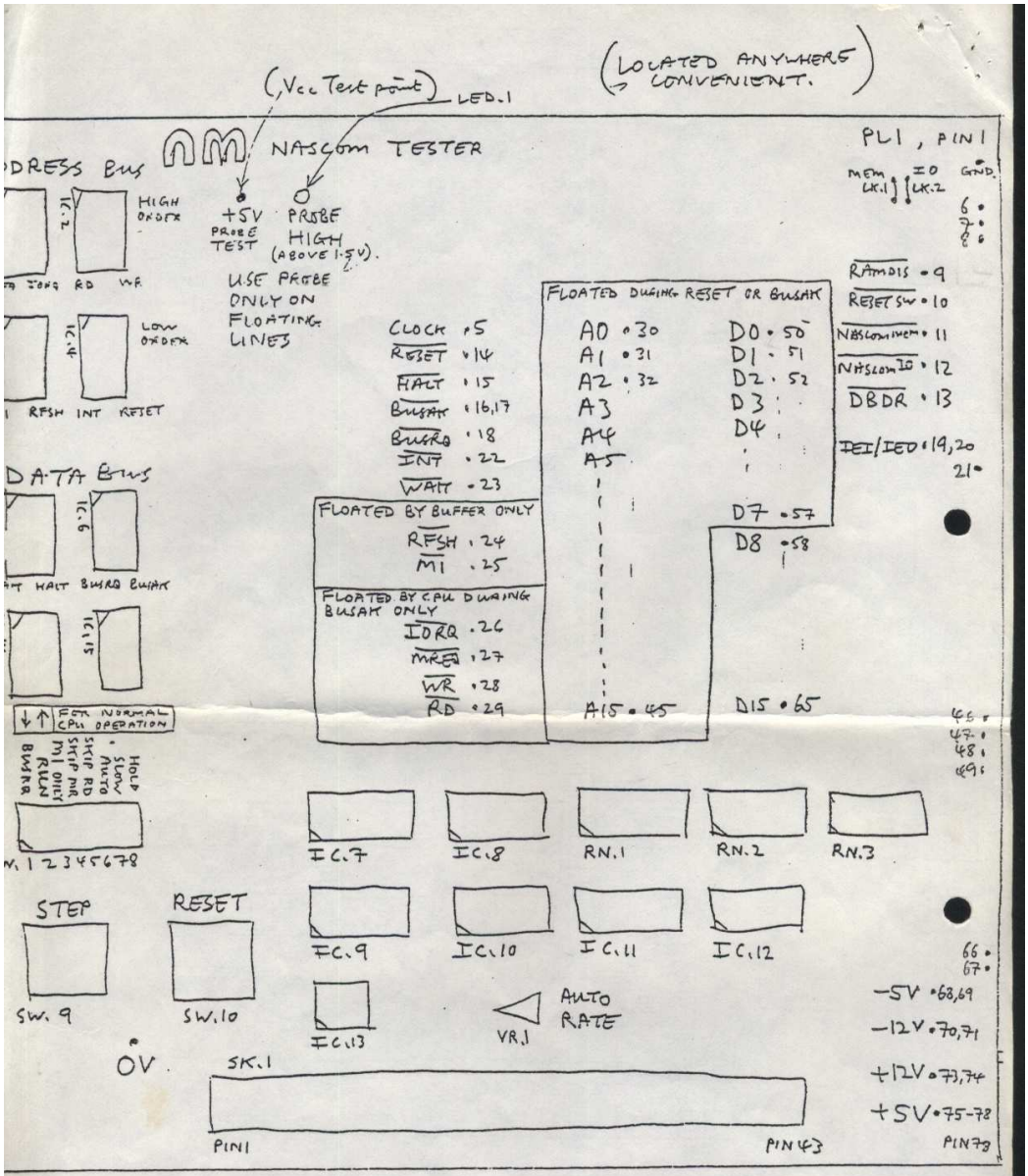
TESTER MK. III

LAYOUT



SUGGESTED SILK-SCREENING

(MINOR COMPONENT DESIGNATIONS TO BE ADDED).

TESTER MK. III

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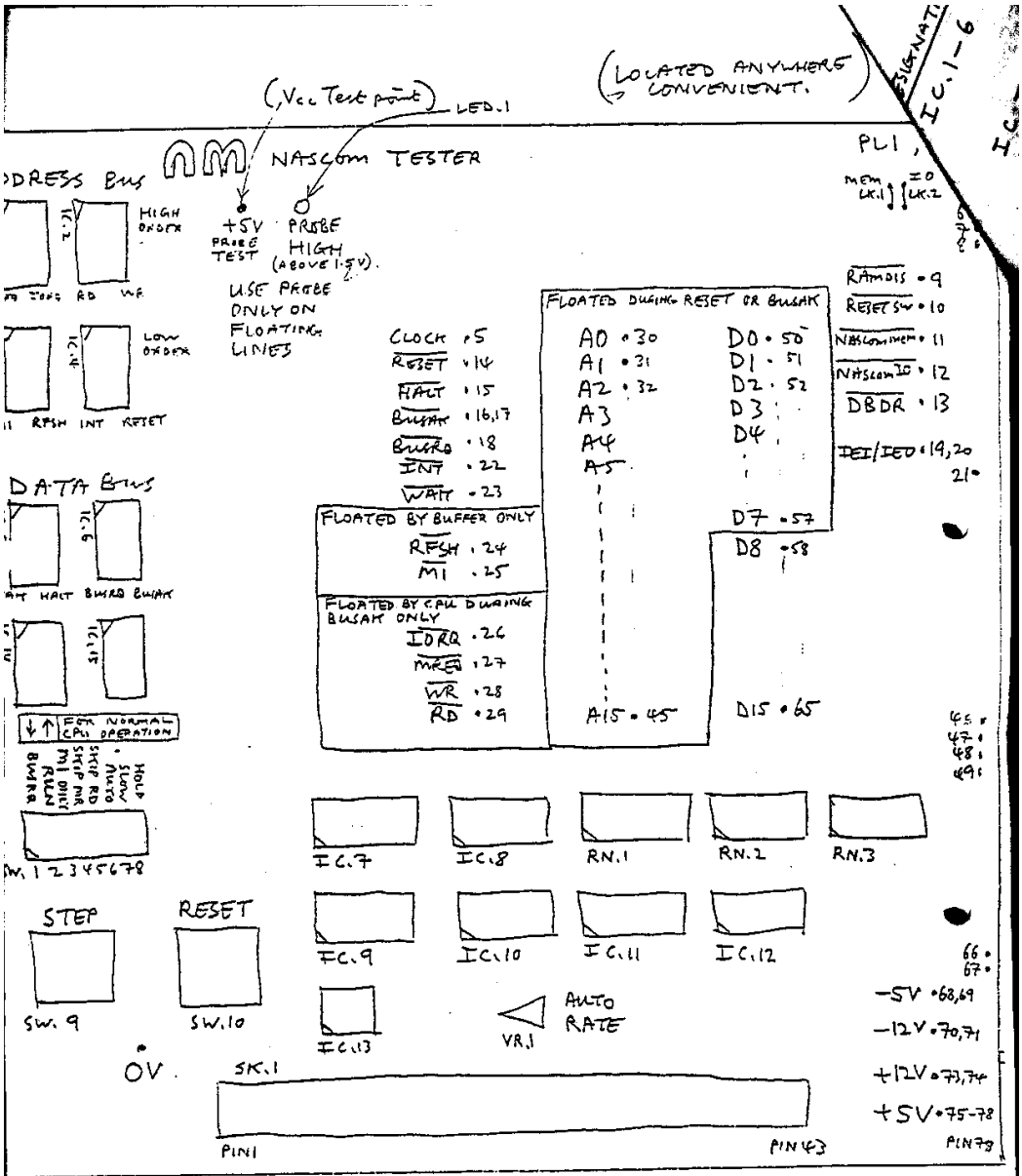
SILK SCREENING



SUGGESTED SILK-SCREENING

(MINOR COMPONENT DESIGNATIONS TO BE ADDED).

DRW/781025 SHT.3

TESTER MK. III

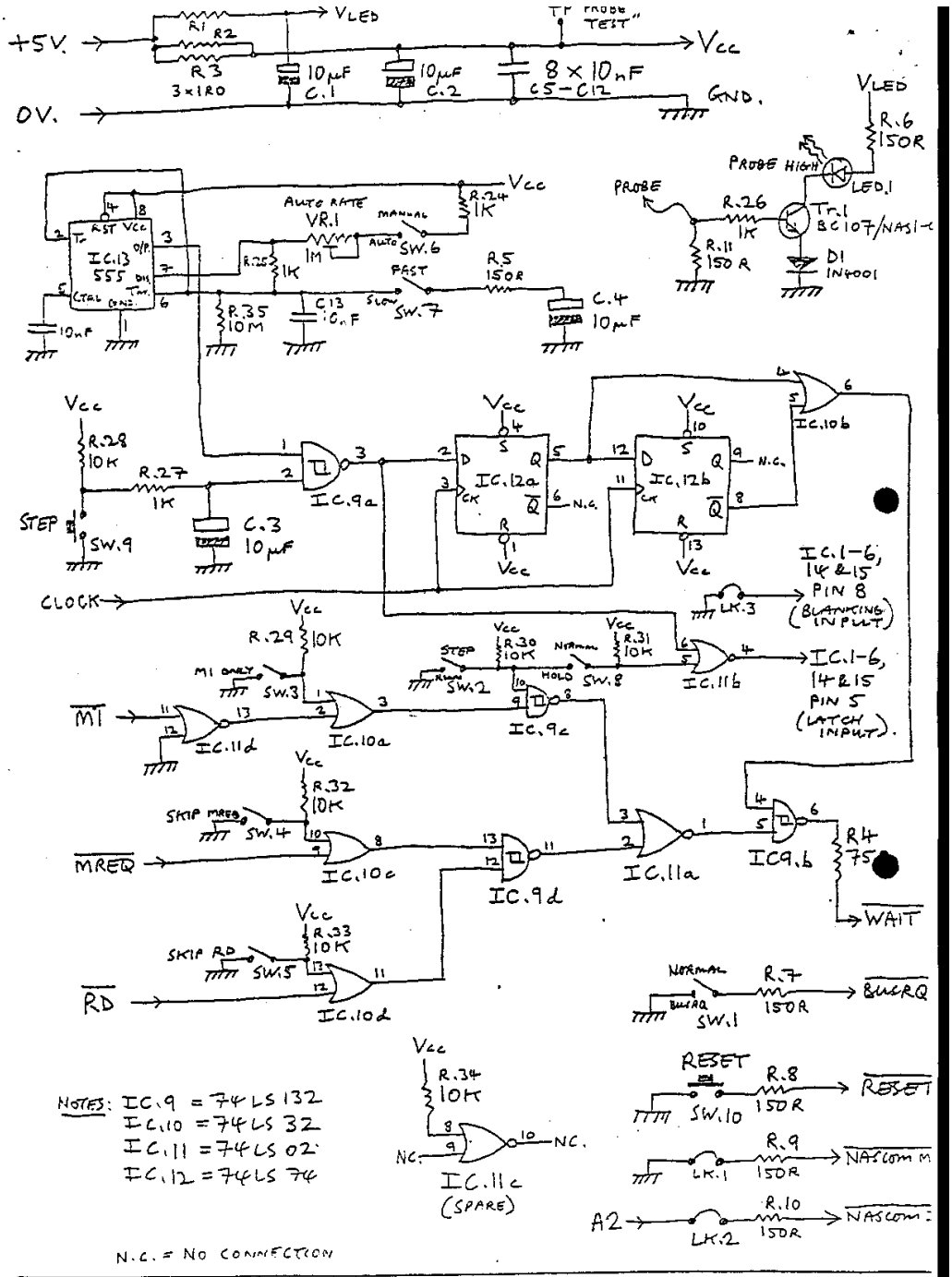
DESIGNATION	NO. OFF	TYPE AND DESCRIPTION	
IC.1–6	6 ×	TIL 311 (Texas) or: RS. 586-734 (£7.05)	HEXADECIMAL DISPLAY
IC.7, 8	2 ×	7407 or 7417	HEX O/C BUFFER
IC. 9	1 ×	74LS132	QUAD 2-IN SCHMITT NAND G
IC. 10	1 ×	74LS 32	QUAD 2-IN OR GATE.
IC. 11	1 ×	74LS 02	QUAD 2-IN NOR GATE.
IC. 12	1 ×	74LS74	DUAL D FLIP-FLOP.
IC. 13	1 ×	555	TIMER
Tr. 1	1 ×	BC 107 or NAS 1-03 :	NPN TRANSISTOR.
LED. 1	1 ×	TIL 209 :	0.125" RED LED.
D. 1	1 ×	IN4001 or IN4002 :	DIODE.
(for SW. 1-8)	1 ×	LOW PROFILE 16 WAY IC. SOCKET.	
(for IC. 1-12 & RN. 1-3)	15×	LOW PROFILE 14 WAY IC. SOCKET.	
(for IC. 13)	1 ×	LOW PROFILE 8 WAY IC. SOCKET.	
SKT. 1	1 ×	VERO 14-0996F : 42 WAY PCB. EDG CONNECTOR WITH MINIWRAP PINS.	
(for SKT. 1)	2 ×	VERO 41-0213E : END BRACKET.	
(ditto.)	2 ×	0.125" (or 3 mm) BOLT, 0.375" (or 10 mm.) LONG	
(")	2 ×	NUT (FOR ABOVE).	
(")	4 ×	PLAIN WASHER. (FOR ABOVE).	
(")	2 ×	SPRING OR STAR WASHER (FOR ABOVE).	
(PROBE)	1 ×	RS. 423-778 :	RED PROBE (£0.5
(ditto.)	6"	RS. 357-081 :	YELLOW EXTRA-FLEXIBLE (£1.09 for 25m.)
(for A0-A15 from Skt. 1)	2 metres ×	SELF FLUXING, POLYURETHANE COATED 0.125 mm. DIA WIRE. (RS. 357-716 FOR 500g. REEL).	

DESIGNATION	NO. OFF	TYPE AND DESCRIPTION
SW. 1–8	1 ×	ERG 'SPECTRA DIL' SWITCH TYPE SDS 8. (8 WAY SINGLE THROW DIL. SWITCH; £88 per 1 — from: Apex, Farnell, Intel, Lock, Roxburgh; or: RS. 339-702 (£1.63).
SW. 9	1 ×	OSMOR PCB. MOUNTING PUSH BUTTON SWITCH, 0.6" SQUARE; WHITE, WITH BLACK LEGEND: PREFERABLY 'STEP' (OTHERWISE 'S' OR BLANK)
SW. 10	1 ×	ditto. but RED, WITH WHITE LEGEND PREFERABLY 'RESET' (OTHERWISE 'R' OR BLANK).
(PCB)	1 ×	PRINTED CIRCUIT BOARD; 8" × 8" DOUBLE SIDED, THROUGH-HOLE-PLATED, SOLDER RESIST BOTH SIDES, SILK SCR PRINTED (YELLOW), GOLD PLATED FINGER ON SOLDER SIDE, SLOTTED, ETC (AS PER NASCO GENERAL SPEC)
(Test Points)	72 ×	(RS. 433-854: AS USED ON NASCO-1 SINGLE SIDED 0.04" DIA TERMINAL P
RN. 1–3.	3 ×	RS. 140-063: 47K RESISTOR NETWORK (or from BECKMAN — NO FURTHER INFORMATION).
VR. 1	1 ×	RS. 185-498: 1M CERMET OPEN MINIATURE POTENTIOMETER. (£
R. 1–3	3 ×	RS. 147-597: 1RO 0.5W METAL FILM RESISTOR. (£0.39 for 10).
R. 4	1 ×	75R RESISTOR, 5%, 0.25W.
R. 5–11	7 ×	150R " " "

DESIGNATION	NO. OFF.	TYPE AND DESCRIPTION
R.12–23	12 x	560 R RESISTOR, 5%, 0.25 W.
R.24–27	4 x	1K0 " " "
R.28–34	7 x	10K " " "
R.35	1 x	10M " " "
C.1–4	4 x	10 µF., 15V (or more) TANTALUM BEAD ELECTROLYTIC CAPACITOR.
C.5–14	10 x	10 nF. DISC CERAMIC CAPACITOR.

NOTE

IC.14 & 15 (AND SOCKETS) NOT REQUIRED AT PRESENT AND NOT LISTED ABOVE (WIRING PROVIDED IN CASE USEFUL IN FUTURE FOR 16 BIT MPU's, GRAPHICS BDS, ETC.).



NOTES: IC.9 = 74LS132
IC.10 = 74LS 32
IC.11 = 74LS 02
IC.12 = 74LS 74

N.C. = NO CONNECTION

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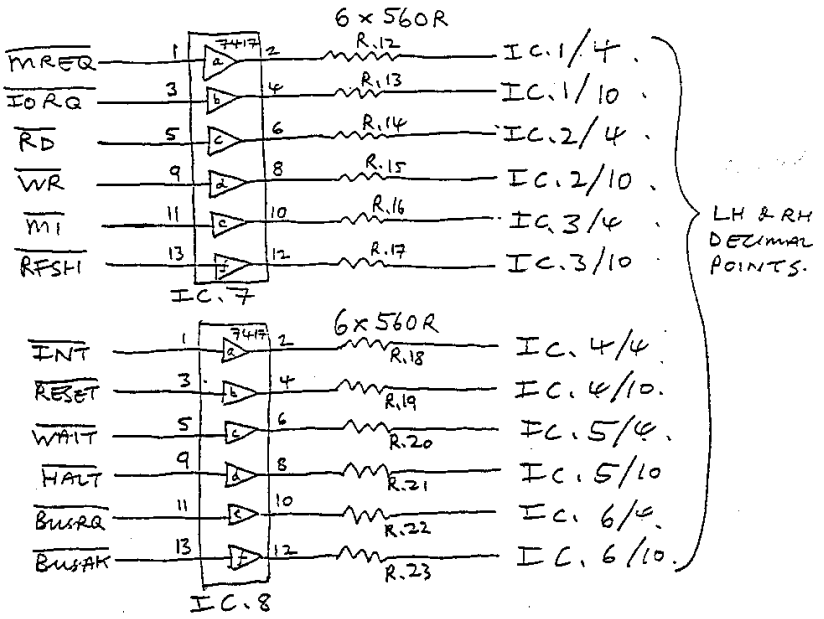


NOTE: IC.1/4 = IC.1 PIN 4.

THE REMAINDER OF THE CIRCUIT DIAGRAM IS IN TABULAR FORM:- (ALL ITEMS ON A LINE ARE CONNECTED)

V_{LED}, IC.1/1, IC.2/1, IC.3/1, IC.4/1, IC.5/1,.
V_{LED}, IC.6/1, IC.14/1, IC.15/1.
V_{cc}, IC.1/14, IC 2/14, IC.3/14, IC.4/14, IC.5/14.
V_{cc}, IC.6/14, IC.7/14, IC.8/14, IC.9/14, IC.10/14,
V_{cc}, IC.11/14, IC.12/14, IC.13/8, IC.14/14, IC.15/14
GND, IC.1/7, IC.2/7, IC.3/7, IC.4/7, IC.5/7,
GND, IC.6/7, IC.7/7, IC.8/7, IC.9/7, IC.10/7,
GND, IC.11/7, IC.12/7, IC.13/1, IC.14/7, IC.15/7.
V_{cc}, RN 1/14, RN 2/14, RN 3/14.

TESTPOINT	PL.1	SK.1	OTHER CONNECTIONS	
GND.	1,2,3,4	40,42,43	(See above)	*(See Sheet 11
CLOCK	5	38	IC.12/3, IC.12/11.	
$\overline{\text{RAMDIS}}$	9			
$\overline{\text{RESET SW.}}$	10			
$\overline{\text{NASCOM MEM}}$	11		R.9	
$\overline{\text{NASCOM IO}}$	12		R.10	
$\overline{\text{DBDR}}$	13			
$\overline{\text{RESET}}$	14	34	IC.8/3, R.8	
$\overline{\text{HALT}}$	15	31	IC.8/9.	
$\overline{\text{BUSAK}}$	16,17	36	IC.8/13.	
$\overline{\text{BUSRQ}}$	18	35	IC.8/11, R.7	
IEI/IEO	19,20			
$\overline{\text{INT}}$	22	33	IC.8/1	
$\overline{\text{WAIT}}$	23	32	IC.8/5, R.4	

NB: FOR RESISTOR CONFIGURATION CROSS CHECK THE ABOVE WITH SHT. 7 & 8

TEST POINT	PL. 1	SH. 1	OTHER CONNECTIONS
$\overline{RFSH}$	24	30	IC. 7/13, IC. 11/9, RN. 3/7.
$\overline{M1}$	25	28	IC. 7/11, IC. 11/11, RN. 3/8.
$\overline{IORQ}$	26	29	IC. 7/3, RN. 3/9.
$\overline{MREQ}$	27	27	IC. 7/1, IC. 10/9, RN. 3/10.
$\overline{WR}$	28	26	IC. 7/9, RN. 3/11.
$\overline{RD}$	29	25	IC. 7/5, IC. 10/12, RN. 3/12
A0	30	21	IC. 4/3, RN. 1/1.
A1	31	23	IC. 4/2, RN. 1/2.
A2	32	24, 39	IC. 4/13, RN. 1/3, LK. 2.
A3	33	22	IC. 4/12, RN. 1/4.
A4	34	19	IC. 3/3, RN. 1/5
A5	35	18	IC. 3/2, RN. 1/6
A6	36	17	IC. 3/13, RN. 1/7
A7	37	16	IC. 3/12, RN. 1/8
A8	38	15	IC. 2/3, RN. 1/9
A9	39	12	IC. 2/2, RN. 1/10
A10	40	14	IC. 2/13, RN. 1/11
A11	41	13	IC. 2/12, RN. 1/12
A12	42	9	IC. 1/3, RN. 1/13
A13	43	10	IC. 1/2, RN. 3/4
A14	44	11	IC. 1/13, RN. 3/5
A15	45	20	IC. 1/12, RN. 3/6
D0	50	1	IC. 6/3, RN. 2/1
D1	51	2	IC. 6/2, RN. 2/2
D2	52	4	IC. 6/13, RN. 2/3
D3	53	6	IC. 6/12, RN. 2/4
D4	54	5	IC. 5/3, RN. 2/5
D5	55	3	IC. 5/2, RN. 2/6

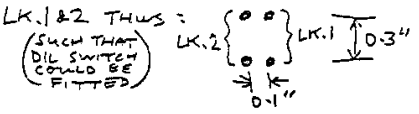
SUGGEST

FINISHED HOLE DIAMETERS : { IC SKT's, SW1-8 AND THRU' HOLES: 0·03
ALL OTHER COMPONENTS: 0·04"
SKT.1 MOUNTING HOLES: 0·125" m

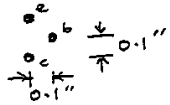
COMPONENT LEAD SPACINGS :-

R.1-3, D1: 0·7"
OTHER R's: 0·5"
LK.3: 0·3"
ALL CAPACITORS: 0·2"
LED.1 : 0·1"
IC. SOCKETS AND SW.1-8 : 0·3" × 0·1" units.

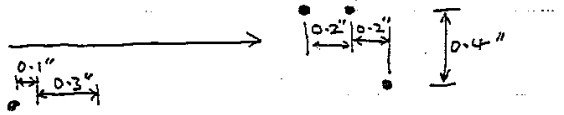
LK.1&2 THUS: (SUCH THAT DIL SWITCH COULD BE FITTED)



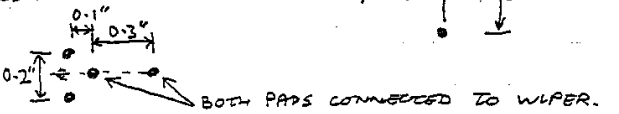
TR.1 THUS: (MAY BE ROTATED)



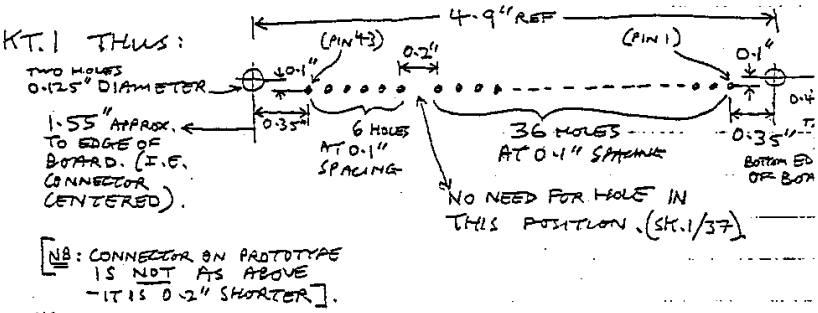
SW.9&10 THUS:



RV.1 THUS:



SKT.1 THUS:



[NB: CONNECTOR ON PROTOTYPE IS NOT AS ABOVE - IT IS 0·2" SHORTER].

NOTE 1: ALL (14) HOLES FOR IC. SOCKETS BENEATH IC.1-6 TO BE DRILLED. (DESPITE MISSING PINS ON TIL 311).

NOTE 2: ALL VIEWS ABOVE ARE FROM THE SOLDER SIDE WITH THE PCB EDGE CONNECTOR ON THE LEFT.

NOTE 3: FOR COMMENTS ON PROTOTYPING AREA AND TEST POINT POSITIONING SEE SHT. 2

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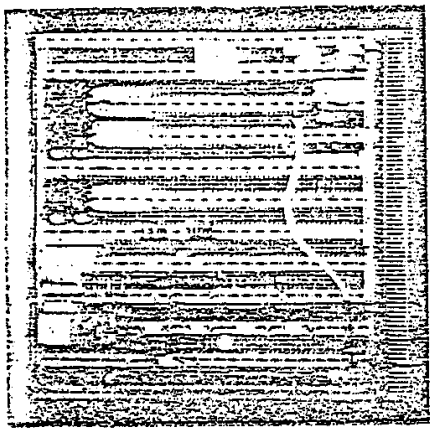
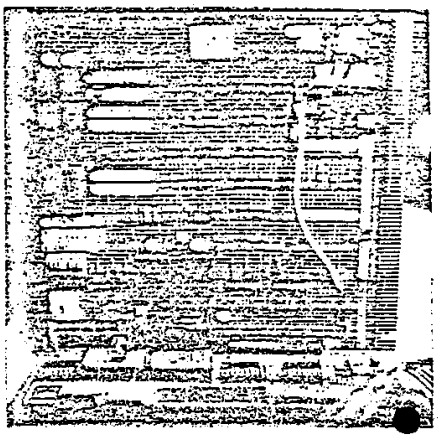
TESTER MK. III

DRILLING INFO



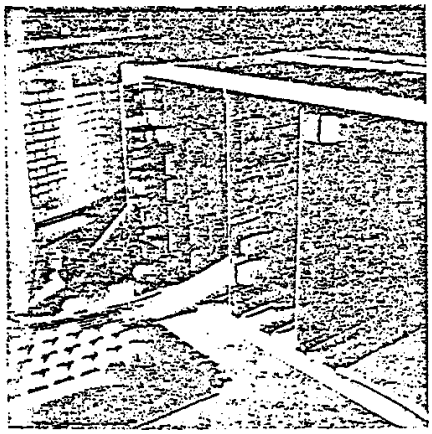
TESTER MK II

@ 25.10.78



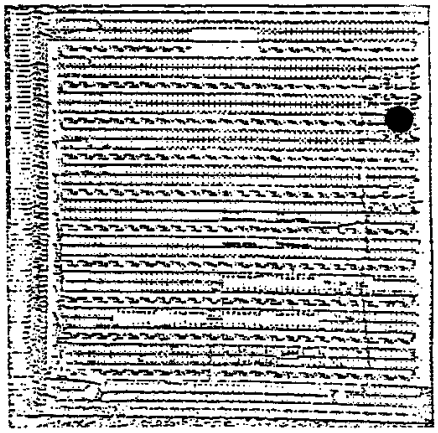
TESTER MK II (IN USE ON NASCOM 1)

@ 25.10.78.



TESTER MK II (INSIDE ON PROTOTYPE WIRING)

@ 25.10.78.



TESTER MK. II (REAR) (PROTOTYPE WIRING).

@ 29.10.78

RE: TESTER MK. III

DRW/781029 SHT 1 OF

PHOTOGRAPHS OF

NASCOM FLOAT AND STEP DISPLAY TESTER EX.1

PURPOSE

To assist in the diagnosis of hardware faults (especially those preventing a correct monitor reset sequence).

DESCRIPTION

The device plugs into the 43 way edge connector on the NASCOM I and continuously displays the state of the address and data busses on the 7-segment displays and most of the control signals on single led's. One switch is provided (on the $\overline{\text{Bus RQ}}$ line) to float the 28 tristate lines and another to enter a "wait" condition so as to freeze the system during any machine cycle. One push button is provided for 'reset' (so that the normal NASCOM keyboard need not be connected) and another to 'step' from one machine cycle to the next (hardware single step feature). A probe is provided to apply a low logic level to test points on each of the 28 tristate lines (for use only in the 'float' condition).

WARNINGS 0. check power supply 5V.O/P before use.

1. Due to non-availability of the correct devices standard B.C.D. display driver I.C.'s are used so that the hexadecimal digits A - F are represented by special 'chance' symbols (as shown on label). Note that 'no segment lit' means F hexadecimal (or 1111 binary) and not necessarily that the lines are floating.

2. There are no pull-up or pull down resistors on the tristate Bus lines. The unit relies on the internal TTL gate pull-up's in the display driver IC's to indicate 'all 1's' when the Busses are 'floating'. (Inputs about + 1.5 to 2.0v on a meter).

3. As this unit applies a standard TTL load to most CPU lines some of them will be technically overloaded and out of spec. Despite this, no problem has yet been found to arise (even at 4 MHz C.P.U. clock rate).

4. It is advisable to remove the PIO chip before testing a NASCOM 1 with this unit (it may affect the data Bus during 'float').

5. This device takes about 0.4A from the NASCOM power supply. This should not however affect circuit operation.

6. The following 2 C.P.U. lines have no display device:-
($\overline{\Phi}$ (clock) { - check with 'scope.
{ - also used by 'wait' circuit)
($\overline{NMI}$ - not available on edge connector)

7. The MEMEXT and $\overline{IOEXT}$ lines are linked on the edge connector (to GND. and A2 respectively) such that the NASCOM 1 links may be in either 'INT' or 'EXT' positions.

8. When the address bus and 4 tristate control lines are floating it is possible that the data bus is being fed from memory. E.G. if both RD and MREQ are made active low (or treated as such by IC44/45) then the contents of address location FFF will probably be read onto the data Bus. To check that a line is floating measure the D.C. potential:- Below 1.0V = LOW; 1.5 to 2.5V=floating; 3.0V to 5V = high. (take care not to short the meter/scope probe to other test points)(IC. pins etc.) A floating line will be pulled down to 0V. by a current of 1 to 2 MA approx. (due to TTL devices on test unit) and pulled up to + 5V by a leakage current around 1 μ A.

SPECIAL FEATURES

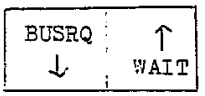
1. At any time all the display device segments may be tested by putting the probe on the 'segment test' test point.

2. At any time the '$\overline{int}$' line may be tested by putting the probe on the '$\overline{INT}$' test point. (no other response is expected as the CPU is unlikely to be programmed to accept an interrupt). All other 'Pull-down' input lines to the CPU are tested with the switches, etc. provided - except $\overline{NMI}$)

3. If the probe is put on a source of + 5V at low impedance ther the 'probe high' led will light. If this happens on one of t test points (giving full brightness) a short to +5V is indicated. The 150 Ω resistor in series w th the probe is likely to pull a normal logic high down sufficiently to ligh the led only dimly.

4. For safety all 'outputs' from the unit have series resistors: 150Ω for $\overline{\text{Bus RQ}}$' switch and 'reset' switch and 82 Ω in series with the wait O/P from IC.7.

5. For normal NASCOM 1 operation the switches should be as shown here:-



6. To 'float' ~~for~~ put $\overline{\text{BUS RQ}}$' switch up (and push 'STEP' if 'WAIT' switch is down).

7. To 'WAIT' (and to use 'STEP') push both switches down.

8. Note that the tristate lines should also be floating while the 'reset' switch is held down.

9. Note that the 'RFSH' led should be out in any 'WAIT' state.

SUGGESTED TEST SEQUENCE

1. Fit unit on NASCOM 1 (without PIO or keyboard).
2. Switch on power (+ 5V already tested).
3. Push both switches up.
4. Push 'reset' button. $\overline{\Phi}$
5. Check presence of CPU (clock) signal
6. All 28 tristate lines should now be floating.
   Both green led's should be lit. (If not ⟶ Fault).
   No other led's or segments may be lit (the only ones that are permitted with a floating Bus are 'wait' and 'halt').
7. If any segments or other led's are lit a short circuit probably exists between the indicated CPU line and some other point (not a CPU line).

   Repair Fault (remove short or replace faulty IC) before proceeding.
8. If NO segments or other led's are lit use the probe on test points as follows:-

   (a) $\overline{\text{INT}}$ (Pull-down line)
   (b) $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MREQ}}$, $\overline{\text{IORQ}}$
   (c) Address bus: A15 ⟶ A0
   (d) Data bus: D7 ⟶ D0

   Then push 'reset' button
   Then push down 'wait' switch

9. For each of the above 31 operations only the relevant led should light or display appear (7, B, D, E HEX = Ø111, 1Ø11, 11Ø1, 111Ø binary).
If there is any discrepancy a fault exists. A short circuit between any two CPU lines will be immediately apparent as both corresponding Led's/Displays will change together.
Repair any fault before proceeding.

10. If no fault has yet been found then open (rather than short) circuits are likely.
Push both switches down
Push 'reset' button
Check display against reset sequence listing
(address bus = ØØØØ; data bus = 31 and controls 'M1' 'MREQ' and 'RD').
Push 'step' button
Check displays again
Repeat these last two items until any discrepancy is found between the display and the listing. * A bit or line shown 'low' on the listing but 'high' on the display indicates an open circuit.

11. If no discrepancy is found by this method:-
Put 'wait' switch up
Push 'reset' switch

12. If no correct reset occurs despite all above testing fault must lie either in an exceptionally slow memory(try 1MHz CPU clock) or in a signal/bit/line that is rarely affected by above tests. Contact D.R.W.

AFTERTHOUGHTS

1. It is assumed that the correct VDU random character display exists before testing begins. (I.E. any number/character generator faults, etc. already repaired).

2. * Incorrect data Bus display during a 'RD' operation (whether M1, MREQ or IORQ etc.) may indicate faulty address decoding or RD/WR gating logic on the C.P.U. board. If more than 1 bit is wrong check round I.C.'s 36, 44 and 45 with a logic probe.

3. Please let D.R.W. know of any comments/Suggested improvements (preferably in writing).

David R. Wadham

David R. Wadham
12-6-78